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Abstract
There are tow major techniques in the wireless LAN systems: the Orthogonal Frequency Division Multiplex (OFDM) and the Spread Spectrum system techniques. The OFDM system was proposed for its efficiency on eliminating the effects of multipath fading and impulse noise. However, it is crucial to obtain the optimum sampling phase for its sensitive to the synchronization errors. It needs a well symbol synchronization scheme to increase the system performance. In this paper, we propose a symbol timing recovery scheme for the OFDM systems. In our scheme, a forgetting factor and adjustable threshold scheme on finding the optimal symbol timing is used to reduce the hardware complexity for the systems.
Finally, we have designed and integrated symbol timing recovery device of 802.11a and 802.11b into an IEEE 802.11 multimode symbol timing recovery processor. Our proposed architecture can be used in the symbol timing recovery of 802.11a/b/g system. The proposed architecture is implemented by UMC 0.18um CMOS technology and its performance is showed as the chip area (gate counts).
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